AMENDMENTS TO THE CLAIMS

1-30. (Canceled)

31. (Currently Amended) A differential driver circuit comprising:

an output driver circuit, including:

differential amplifier circuitry;

a first variable resistance circuit that is coupled to the differential amplifier circuitry; and

a second variable resistance circuit that is coupled to the differential amplifier circuitry; and

a feedback circuit that is coupled to the first and second variable resistance circuits, wherein a source resistance of the output driver circuit appears to a load as substantially similar to a termination resistance of the load,

wherein the feedback circuit includes a third variable resistance circuit,

the third variable resistance circuit includes a replica of the first variable resistance circuit,

the third variable resistance circuit is coupled to the first variable resistance circuit,

the feedback circuit further includes a fourth variable resistance circuit,

the fourth variable resistance circuit includes a replica of the second variable resistance circuit,

the fourth variable resistance circuit is coupled to the second variable resistance circuit, and

wherein the feedback circuit further includes:

a transistor that is coupled between the third variable resistance circuit and the fourth variable resistance circuit;

a first operational amplifier circuit that is coupled between the transistor and the third variable resistance circuit; and

a second operational amplifier circuit that is coupled between the transistor and the fourth variable resistance circuit.

32. (Previously Presented) The differential driver circuit of Claim 31, wherein the feedback circuit includes a scaled replica of a leg of the output driver circuit.

33. (Previously Presented) The differential driver circuit of Claim 31, wherein the feedback circuit is configured to adjust the first variable resistance circuit and the second variable resistance circuit to track a change in the termination resistance, such that the source resistance tracks the change in the termination resistance.

34. (Previously Presented) The differential driver circuit of Claim 31, wherein the differential amplifier circuitry includes:

a first transistor that is coupled between the first variable resistance circuit and a first output node;

a second transistor that is coupled between the first variable resistance circuit and a second output node;

a third transistor that is coupled between the second variable resistance circuit and the first output node; and

a fourth transistor that is coupled between the second variable resistance circuit and the second output node.

35. (Previously Presented) The differential driver circuit of Claim 31, wherein the first variable resistance circuit includes a transistor having a drain that is coupled to the differential amplifier circuitry and a gate that is coupled to the feedback circuit.

36. (Previously Presented) The differential driver circuit of Claim 35, wherein the feedback circuit is configured to adjust an on-resistance that is associated with the transistor.

37. (Previously Presented) The differential driver circuit of Claim 35, wherein

the first variable resistance circuit further includes a resistor that is coupled in parallel with the transistor.

38. (Previously Presented) The differential driver circuit of Claim 35, wherein the second variable resistance circuit includes another transistor having a drain that is coupled to the differential amplifier circuitry and a gate that is coupled to the feedback circuit.

39. (Previously Presented) The differential driver circuit of Claim 38, wherein the feedback circuit is configured to modulate the transistor and the other transistor.

40. (Previously Presented) The apparatus of Claim 31, wherein the output driver circuit further includes a current source circuit that is coupled to the feedback circuit and the first variable resistance circuit.

41. (Previously Presented) The apparatus of Claim 40, wherein the output driver circuit further includes a current sink circuit that is coupled to the feedback circuit and the second variable resistance circuit.

42. (Canceled)

43. (Canceled)

44. (Canceled)

45. (Currently Amended) The apparatus of Claim 31[[44]], wherein the first operational amplifier circuit is configured to adjust a resistance that is associated with the first variable resistance circuit and a resistance that is associated with the third variable resistance circuit, and

wherein the second operational amplifier circuit is configured to adjust a resistance that is associated with the second variable resistance circuit and a resistance that is associated with the fourth variable resistance circuit.

46. (Currently Amended) The apparatus of Claim 31[[44]],

wherein the output driver circuit further includes a first current source circuit that is coupled to the first variable resistance circuit,

the feedback circuit further includes:

a replica resistor that is coupled in parallel with the transistor;

a second current source circuit that is a replica of the first current source circuit; and

a third operational amplifier circuit that is coupled to the first variable resistance circuit, the third variable resistance circuit, and the transistor, and

wherein the third operational amplifier circuit is configured to adjust the transistor such that the first current source and the second current each provide an approximately constant current.

47. (Canceled)

48. (Canceled)

49. (Currently Amended) A differential driver circuit comprising:

an output driver circuit, including:

differential amplifier circuitry that is configured to provide a differential output signal in response to a differential input signal;

a first variable resistance circuit that is configured to vary a resistance that is associated with the first variable resistance circuit in response to a first control signal; and

a second variable resistance circuit that is configured to vary a resistance that is associated with the second variable resistance circuit in response to a second control signal; and

a feedback circuit that is configured to provide the first control signal and the second control signal, wherein a source resistance of the output driver circuit appears to a load as substantially similar to a termination resistance of the load,

wherein the output driver circuit is further configured to provide a monitor signal,

the feedback circuit includes:

a third variable resistance circuit that is configured to vary a resistance that is associated with the third variable resistance circuit in response to the first control signal,

wherein the third variable resistance circuit is a replica of the first variable resistance circuit;

a fourth variable resistance circuit that is configured to vary a resistance that is associated with the fourth variable resistance circuit in response to the second control signal, wherein

the fourth variable resistance circuit is a replica of the second variable resistance circuit;

a transistor that is coupled between the third variable resistance circuit and the fourth variable resistance circuit;

a first operational amplifier that is configured to provide the first control signal;

a second operational amplifier that is configured to provide the second control signal; and

a third operational amplifier circuit that is coupled to the first variable resistance circuit, the third variable resistance circuit, and the transistor, wherein

the third operational amplifier circuit is configured to modulate the transistor in response to the monitor signal such that the first current source circuit and the second current source circuit each provide approximately constant current~~The differential driver circuit of Claim 48~~,

wherein the output driver circuit further includes:

a first current source circuit that is coupled to the first variable resistance circuit and the feedback circuit; and

a first current sink circuit that is coupled to the second variable resistance circuit and the feedback circuit,

the feedback circuit further includes:

a second current source circuit that is a replica of the first current source circuit;

a second current sink circuit that is a replica of the first current sink circuit;

a fourth operational amplifier circuit that is configured to bias the first and second current source circuits in response to a first upper reference signal and a first feedback signal; and

a fifth operational amplifier circuit that is configured to bias the first and second current sink circuits in response to a first lower reference signal and a second feedback signal,

the transistor is coupled between a first feedback node and a second feedback node,

the first operational amplifier circuit is configured to provide the first control signal in response to a third feedback signal that is received at the first feedback node and a second upper reference signal, and

wherein the second operational amplifier circuit is configured to provide the second control signal in response to a fourth feedback signal that is received at the second feedback node and a second lower reference signal.

50. (Canceled)

51. (Canceled)

52. (Canceled)

53. (Canceled)

54. (Currently Amended) A differential driver circuit, comprising:

an output driver circuit, including:

differential amplifier circuitry;

a first variable resistance circuit that is coupled to the differential amplifier circuitry; and

a second variable resistance circuit that is coupled to the differential amplifier circuitry; and

a feedback circuit that is configured to control a resistance that is associated with the first variable resistance circuit and a resistance that is associated with the second variable resistance circuit such that a source resistance of the output driver circuit tracks the termination resistance,

wherein the output driver circuit further includes:

a current source transistor that is arranged to provide a current responsive to a bias signal, wherein the current source transistor operates in a saturation region of operation or an active region of operation, the first variable resistance circuit is coupled between the current source circuit and the differential amplifier circuitry, and wherein the first variable resistance circuit is arranged to receive the current.

55. (Previously Presented) The differential driver circuit of Claim 54, wherein the first variable resistance circuit includes:

a transistor; and

a resistive element that is coupled in parallel with the transistor.

56. (Currently Amended) A differential driver circuit, comprising:

an output driver circuit, including:

differential amplifier circuitry;

a first variable resistance circuit that is coupled to the differential amplifier circuitry; and

a second variable resistance circuit that is coupled to the differential amplifier circuitry; and

a feedback circuit that is configured to control a resistance that is associated with the first variable resistance circuit and a resistance that is associated with the second variable resistance

circuit such that a source resistance of the output driver circuit tracks the termination resistance~~The differential driver circuit of Claim 54~~, wherein

the feedback circuit includes:

a third variable resistance circuit;

a fourth variable resistance circuit;

a transistor that is coupled between the third variable resistance circuit and the fourth variable resistance circuit;

a first op amp circuit that is coupled between the transistor and the third variable resistance circuit; and

a second op amp circuit that is coupled between the transistor and the fourth variable resistance circuit.

57. (Currently Amended) The differential driver circuit of Claim 56[[54]], wherein

the output driver circuit further includes:

a current source transistor that is arranged to provide a current responsive to a bias signal, wherein the current source transistor operates in a saturation region of operation or an active region of operation, the first variable resistance circuit is coupled between the current source circuit and the differential amplifier circuitry, and wherein the first variable resistance circuit is arranged to receive the current.

58. (Previously Presented) The differential driver circuit of Claim 54, wherein

the first variable resistance circuit includes a transistor, the transistor includes a gate, and wherein the feedback circuit is arranged to control the resistance that is associated with the first variable resistance circuit by providing a first control signal to the gate of the transistor such that the transistor is biased in a linear region of operation.

59. (Previously Presented) The differential driver circuit of Claim 58, wherein

the second variable resistance circuit includes another transistor, the other transistor includes a gate, and wherein the feedback circuit is arranged to control the resistance that is associated with

the second variable resistance circuit by providing a second control signal to the gate of the other transistor such that the other transistor is biased in the linear region of operation.